Vertical FET's in GaAs

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Abstract—**Vertical FET's in GaAlAs material systems have been fabricated. The present structure makes possible extremely short (less than 1000-Å) channel devices which are beyond the reach of optical lithographic processes. Devices with transconductance g_m as high as 280 mS/mm have been obtained.**

VERTICAL FET IN THE GaAs/GaAlAs MATERIAL SYSTEM

THE INTRODUCTION of DMOS (double-diffused MOS) and VMOS (vertical or V-groove MOS) based on silicon has led to significant improvement in the performance of microwave amplifiers, high-speed logic devices, and especially high voltage switching devices [1]. III-V semiconductor devices offer superior performance due to the high mobility and saturation velocity. The vertical FET structure reported in this work has made possible the fabrication of submicrometer devices without sophisticated submicrometer lithographic processes.

The critical dimension in our devices is defined by the thickness of an epitaxially grown layer and can thus be controlled to a degree of accuracy unattainable in lithographic processes, especially with advanced crystal growth techniques such as molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD). An advantage of vertical FET's is the ability to independently optimize the doping densities of the layers. In addition, the III-V material offers an extra degree of freedom unavailable in Si through the use of heterojunctions. The band discontinuity at a heterojunction can be used to exploit transient electron transport phenomena such as velocity overshoot [2], [3] and ballistic transport [4] to achieve high electron velocity. Moreover, the difference in mobility and band-gap of III-V compounds can be utilized to optimize important parameters such as breakdown voltages in different applications.

In the past few years, short-channel devices have generated considerable interest. However, conventional submicrometer devices often suffer from high source resistance which offsets the advantage gained from the short channel. The vertical FET design presented here makes is possible to embed a thick $n(2 \sim 4 \times 10^{17}\ \mathrm{cm}^{-3})$ layer next to the channel. Thus the source and drain parasitic series resistance can be drastically reduced owing to the removal of the undesirable effect of surface depletion in the channel between the gate edge and the source ohmic contact. However, the reduction of the channel length causes short-channel effects to become more significant. These include a higher current in the subthreshold region and a threshold voltage which depends on the drain voltage. These effects can be reduced by introducing a thin p^+ or n-layer between the channel and the n^+ drain. The penetration of the depletion region from the drain toward the channel is suppressed by such schemes.

The GaAs vertical FET has considerable advantage compared to silicon transistors as far as high-voltage switching applications are concerned. The dominant feature of high power FET design is the minimization of the on resistance subject to the voltage, current, and speed requirements [5], [6]. A lightly doped n^- layer is used on the drain side of the channel region to increase the drain breakdown voltage. At low drain voltage, the resistance of the n^- layer dominates the on characteristics of the device. There is a tradeoff between breakdown voltage and the on-resistance. The on-resistance of such devices increases with increasing drain-source voltage capability. III-V vertical FET structure provides an on-resistance value about six times smaller than Si devices with the same voltage capability because of the high electron mobility.

Vertical FET's were fabricated in the GaAs/GaAlAs material system with both LPE and MBE grown wafers. The structure is shown in Fig. 1(a). The epitaxial layers were successively grown by LPE or MBE on n^+ GaAs substrate with the following compositions: 3-μm $n(1.5 \times 10^{17}\ \mathrm{cm}^{-3})$, 0.15-$\mu$m $p(1 \sim 2 \times 10^{17}\ \mathrm{cm}^{-3})$, 1.5-$\mu$m $n(3 \times 10^{17}\ \mathrm{cm}^{-3})$. Grooves of 2.5-$\mu$m depth were etched with $1:8:8(H_2SO_4:H_2O_2:H_2O)$. $6 \times 10^{12}\ \mathrm{cm}^{-2}$ Si was ion implanted at an energy of 120 keV.

Schottky gates with breakdown voltage of ~ -4 V and reasonably low gate-to-source series resistance ($\sim 1\ \Omega$/mm) were obtained. Following annealing AuGe/Au ohmic contacts were deposited for the drain and souce. Definition of an aluminum gate completed the device.

Interesting results were obtained with the device shown in Fig. 1(a). When operating with the source and drain as shown the drain current-voltage (DC) characteristics are shown in Fig. 2(a) and (b). At zero gate voltage, in Fig. 2(b), the channel is fully depleted and the device is an enhancement-type transistor.

The *I-V* curve (Fig. 2) shows the short-channel characteristics with the combined effect of saturation and punchthrough

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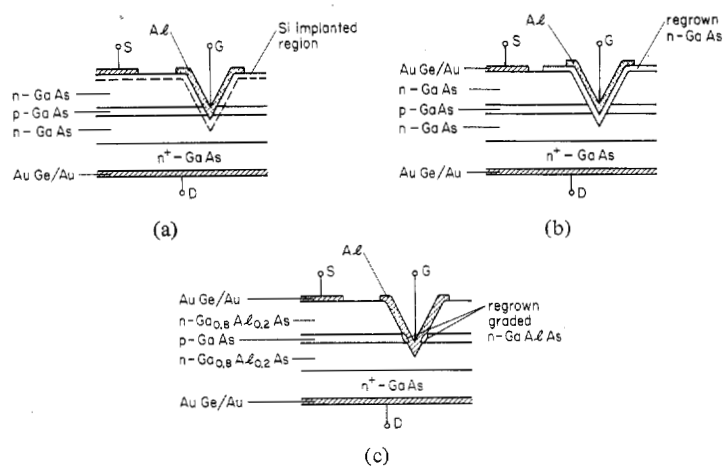

Fig. 1. (a) Schematic drawing of the implanted GaAs vertical MESFET. (b) Schematic drawing of the vertical GaAs MESFET with a grown thin n-FET layer. (c) Schematic drawing of the heterostructure vertical FET with selective lateral growth.

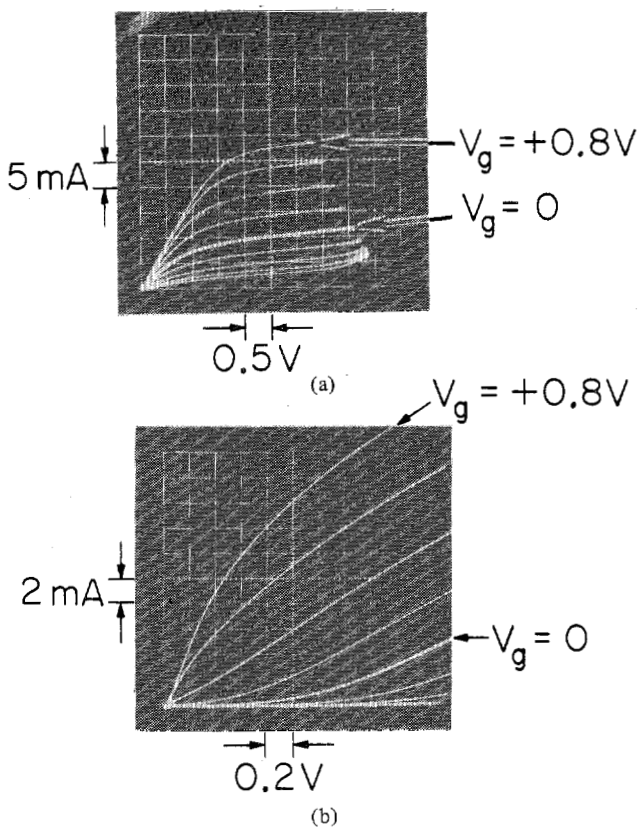

Fig. 2. Drain current–voltage characteristics of the ion-implanted vertical GaAs MESFET's. (a) LPE-grown layers (gate width of 100 μm). (b) MBE-grown layers (gate width of 120μm).

effects. When punchthrough occurs in the channel, electrons can be injected into the depleted channel region and the current is space-charge limited. Under low gate voltages, the space-charge current dominates. However, at higher voltages, the total drain current is the sum of the channel and space-charge-limited current [7]. These give rise to the characteristics as shown in Fig. 2(a) and (b). A typical g_m value is about 250 mS/mm, the highest obtained is 280 mS/mm. These values are as measured values. A correction for the source resistance yields g_m values in excess of 320 mS/mm. It should be noted that no hysteresis has been observed on our FET's.

In a short-channel ion-implanted vertical FET, there exists a practical and important limitation on the device performance. To eliminate the undesirable source-drain punchthrough effect, the doping level in the p-layer has to be high. However, if the doping level N_A is increased beyond 2×10^{17} cm^{-3}, control of the channel doping $N_i - N_A$ becomes difficult. Also, the channel layer will be a highly compensated region which leads to reduced mobility. In addition, a too high implantation dosage will degrade or even destroy the Schottky barrier between the part of the gate overlapping the source and drain. The same problem is found in self-aligned FET's [8]. These considerations lead to an upper limit of about 2×10^{17} cm^{-3} for the p-layer. This problem can be solved by growing a thin ($\approx$50 nm with 2×10^{17} cm^{-3} n$^-$ FET) layer (by MBE or MOCVD) instead of implantation as shown in Fig. 1(b). This completely removes the limitation on the doping level in the p$^+$ and n$^+$ layer. As a result, the Schottky barrier between the gate and the source layer is now higher. An alternative solution is to employ a heterostructure with GaAlAs layers for the source and drain and GaAs for the channel layer. The n GaAs channel layer can now be grown on the p-GaAs by lateral selective area growth using LPE [9] (Fig. 1(c)), as there exists preferential growth over the GaAs surface only when both the GaAs and GaAlAs regions are exposed to a solution of GaAlAs. Very thin layers can be grown in this manner. An additional advantage of this structure is the increased Schottky barrier height between the gate metal and higher gap GaAlAs. Preliminary results from devices resulted in uncorrected g_m values as high as 280 mS/mm.

In conclusion, high transconductance vertical FET's have been fabricated in GaAs/GaAlAs. The use of a vertical structure allows submicrometer devices to be fabricated without sophisticated photolithographic processes. The transistors exhibited high transconductance. Potential applications in high-power high-voltage switching devices and high-speed

devices utilizing heterostructures are currently being investigated. In order to realize this potential, minimization of different parasitics is needed by using fine line lithography in the lateral direction. For high-voltage handling the overlap between the gate and drain should be minimized to eliminate Schottky breakdown.

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